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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,647	04/22/2004	Teck Kheng Lee	2269-4974.1US (00-0693.01	6967

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EXAMINER	
PERKINS, PAMELA E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,647	LEE, TECK KHENG	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/150,901.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/22/04, 11/15/04*. 2/14/05; 5/11/05 6/27/05 11/7/05, 12/12/05, 4/10/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application papers on 22 April 2004. Claims 1-14 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (2003/0134450)

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Referring to claim 1, Lee discloses a method of fabricating an interposer substrate for attaching to an active surface of a semiconductor die having a plurality of

conductive bumps protruding transversely therefrom where a substrate (36') has a first surface and a second surface, the substrate (36') including a dielectric layer and a plurality of conductive elements (44') on the dielectric layer adjacent the second surface; and forming a plurality of recesses (40') the first surface of the substrate (36') and through the dielectric layer to a depth through the dielectric layer, each of the plurality of recesses (40') exposing at least a portion of a contiguous conductive element (44') adjacent the second surface and of a size and configuration to receive the plurality of conductive bumps (60') of the semiconductor die (54') so that the plurality of conductive bumps (60') is substantially received within the plurality of recesses (40') (para. 32-39).

Claim 2. Wherein forming the plurality of recesses (40') comprises forming the plurality of recesses (40') to a depth so that a surface of each of the plurality of conductive bumps (60') will contact the at least a portion of the contiguous conductive element (44') with the active surface of the semiconductor die (54') abutting the first surface of the substrate (36') (para. 41).

Claim 3. Forming at least one opening in the second surface of the substrate in communication with at least one recess of the plurality of recesses (40').

Claim 4. Wherein providing the substrate (36') comprises forming the plurality of conductive elements (44') by at least one of printing conductive ink and etching a conductive layer (para. 32).

Claim 5. Wherein providing the substrate (36') comprises disposing a solder mask (49') over the plurality of conductive elements (44') in a pattern leaving portions of the plurality of conductive elements (44') exposed (para. 34).

Claim 6. Wherein providing the substrate (36') comprises providing the dielectric layer as a flexible polymer material (para. 30).

Claim 7. Wherein providing the substrate (36') comprises providing the substrate (36') to include at least one of BT, FR4 laminate, FR5 laminate and UPILEXO ® (para. 30).

Claim 8. Wherein forming the plurality of recesses (40') comprises collectively configuring the plurality of recesses (40') in a centrally aligned row in the substrate (36') to correspond with a conductive bump (60') configuration on the semiconductor die (54') (Fig. 5; para. 38).

Claim 9. Wherein forming the plurality of recesses (40') comprises collectively configuring the plurality of recesses (40') in a peripheral configuration in the substrate (36') to correspond with a conductive bmp (60') configuration on the semiconductor die (54') (Fig. 5; para. 54).

Claim 10. Wherein forming the plurality of recesses (40') comprises collectively configuring the plurality of recesses (40') in an I-shaped configuration in the substrate (36') to correspond with a bump (60') configuration on the semiconductor die (54') (fig. 4 & 5; para. 35-38).

Claim 11. Wherein forming the plurality of recesses (40') comprises forming the plurality of recesses (40') by at least one of a wet etch, dry etch, mechanical drilling, mechanical punching and laser ablation (para. 32).

Claim 12. Wherein forming the plurality of recesses (40') comprises patterning the plurality of recesses (40'), each substantially with a peripheral shape including at least one of a square, rectangle, circle and oval (para. 33).

Claim 13. Wherein forming the plurality of recesses (40') comprises forming at least one sloped sidewall in each of the plurality of recesses (40') (para. 34).

Claim 14. Wherein forming the plurality of recesses (40') comprises forming at least one sidewall in each of the plurality of recesses (40') to be substantially perpendicular with respect to the first surface of the substrate (36') (para. 34).

Claims 1-3, 5, 8-10, 12 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Greenwood (6,338,985).

Referring to claim 1, Greenwood discloses a method of fabricating an interposer substrate for attaching to an active surface of a semiconductor die having a plurality of conductive bumps protruding transversely therefrom where a substrate (12) having a first surface and a second surface, the substrate (12) including a dielectric layer (15) and a plurality of conductive elements (25) on the dielectric layer (15) adjacent the second surface (col. 4, lines 5-14); and forming a plurality of recesses (32) in the first surface of the substrate (12) and through the dielectric layer (15) to a depth through the dielectric layer (15) (Fig. 5), each of the plurality of recesses (32) exposing at least a portion of a contiguous conductive element (24) adjacent the second surface and of a size and configuration to receive the plurality of conductive bumps (42) of the

semiconductor die (40) so that the plurality of conductive bumps (42) is substantially received within the plurality of recesses (32) (Fig. 7; col. 4, line 65 thru col. 5, line 20).

Claim 2. Wherein forming the plurality of recesses (32) comprises forming the plurality of recesses (32) to a depth so that a surface of each of the plurality of conductive bumps (42) will contact the at least a portion of the contiguous conductive element (24) with the active surface of the semiconductor die (40) abutting the first surface of the substrate (12) (col. 5,lines 4-20).

Claim 3. Forming at least one opening in the second surface of the substrate in communication with at least one recess of the plurality of recesses (32) (Fig. 5; col. 4, lines 15-56).

Claim 5. Wherein providing the substrate (12) comprises disposing a solder mask (34) over the plurality of conductive elements (24) in a pattern leaving portions of the plurality of conductive elements (24) exposed (col. 4, lines 41-56).

Claim 8. Wherein forming the plurality of recesses (32) comprises collectively configuring the plurality of recesses (32) in a centrally aligned row in the substrate (12) to correspond with a conductive bump (42) configuration on the semiconductor die (40) (Fig. 7; col. 5, lines 21-42).

Claim 9. Wherein forming the plurality of recesses (32) comprises collectively configuring the plurality of recesses (32) in a peripheral configuration in the substrate (12) to correspond with a conductive bmp (42) configuration on the semiconductor die (40) (Fig. 7; col. 5, lines 21-42).

Claim 10. Wherein forming the plurality of recesses (32) comprises collectively configuring the plurality of recesses (32) in an I-shaped configuration in the substrate (12) to correspond with a bump (42) configuration on the semiconductor die (40) (Fig. 7; col. 5,lines 4-42).

Claim 12. Wherein forming the plurality of recesses (32) comprises patterning the plurality of recesses (32), each substantially with a peripheral shape including at least one of a square, rectangle, circle and oval (Fig. 5; col. 4, lines 14-39).

Claim 14. Wherein forming the plurality of recesses (32) comprises forming at least one sidewall in each of the plurality of recesses (32) to be substantially perpendicular with respect to the first surface of the substrate (12) (col. 4, lines 14-39).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PEP
24 June 2006

Zandra V. Smith
Supervisory Patent Examiner
26 June 2006